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(54) Process for manufacturing integrated devices having connections on separate wafers and stacking the same

(57) A process for manufacturing an integrated device (36) comprises the steps of: forming, in a first wafer (1) of semiconductor material, integrated structures (3, 4) including semiconductor regions (10, 12-15, 20) and isolation regions (7, 18); forming, on a second wafer (25) of semiconductor material, interconnection structures (28-30, 32) of a metal material including plug elements (32) having at least one bonding region (34) of a metal material capable of reacting with the semiconductor regions (10, 12-15, 20) of the first wafer (1); and bonding the first and second wafers together by causing the bonding regions (34; 70) of the plug elements (32) to react directly with the semiconductor regions so as to form a metal silicide. Thereby, the metallurgical operations for forming the interconnection structures are completely independent of the operations required for processing silicon, so that there is no interference whatsoever between the two sets of operations. In addition, the areas where the two wafers are made may be separate, and the interconnection structures may be made with materials incompatible with silicon processing, without any risk of contamination.

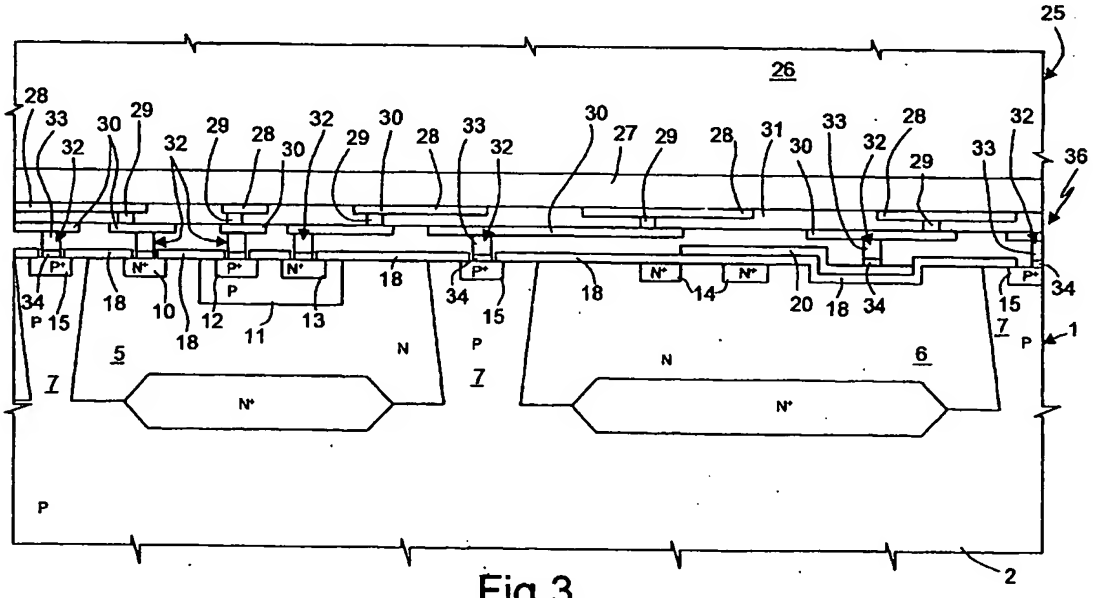

Fig.3

EP 1 219 565 A1

Description

[0001] The present invention refers to a process for manufacturing integrated devices having connections on a separate wafer, and to an integrated device thus obtained.

[0002] As is known, standard processes for manufacturing integrated circuits involve carrying out individual process steps in a sequential way. The manufacture of micro-integrated structures (so-called micro-electromechanical systems, or MEMS) and their control circuits in a same monolithic device has required a certain number of manufacture steps for defining the micro-integrated structures within the process of manufacturing traditional electronic components, with an increase in complexity which is not always sustainable. Consequently, in many cases the choice is made to carry out parallel manufacturing processes to obtain, on one hand, the control circuits, and, on the other, the micro-integrated structures, and at a certain point to bond the obtained structures, so that the two processes may involve only a few non-critical common steps.

[0003] Thereby, it is possible to continue to exploit the potential of planar technology (batch-type processes), whilst the minimum time required for obtaining a finished device (so-called "cycle time") is markedly reduced. In addition, with parallel processing, it is possible to separate parts and processing steps that could lead to contamination.

[0004] Recently a manufacturing process has been proposed (see US-A-5,736,395) based upon parallel manufacture of a first substrate housing an integrated circuit and a second substrate comprising the interconnections for the integrated circuit, and bonding the two substrates together in the final manufacturing steps.

[0005] The separation of the operations for forming the integrated components in a silicon substrate from the operations for forming interconnections enables a simplification of the process as a whole.

[0006] In the parallel process proposed, bonding of the two substrates is obtained by forming, on both substrates, appropriate metal contact regions coated with a bonding layer of a low-melting alloyable metal, for example gold or palladium.

[0007] The need to include steps for depositing and defining the metal contact regions and the bonding layer on top of both substrates is, however, disadvantageous in so far as it does not enable separation of the operations for forming components integrated in the silicon from the metallurgical operations for forming interconnections. Consequently, the techniques for forming the interconnections risk affecting the components that belong to the integrated circuit and may give rise to undesired charging phenomena or to contamination.

[0008] In addition, the described parallel process requires forming through holes in the substrate carrying the interconnections for aligning the two substrates in the bonding step, with an increase in costs and in manufacturing times for forming the corresponding masks and the holes.

[0009] The aim of the present invention is therefore to provide a parallel manufacturing process that eliminates the need to form contact regions and a bonding layer on both substrates, so as to keep the metallurgical operations completely separate from the operations for forming integrated components of semiconductor or insulating material, and to simplify the operations for bonding the two substrates.

[0010] According to the present invention, a process is provided for manufacturing integrated devices, as well as an integrated device thus obtained, as defined in Claim 1 and Claim 13, respectively.

[0011] For a better understanding of the present invention, preferred embodiments thereof are now described, purely to provide nonlimiting examples, with reference to the attached drawings, wherein:

- Figure 1 shows a cross-section of a first wafer housing electronic components for implementing the parallel manufacturing process according to the invention;
- Figure 2 shows a cross-section of a second wafer housing interconnections for the components of Figure 1;
- Figure 3 shows a cross-section of a composite wafer obtained by bonding the wafers of Figures 1 and 2;
- Figure 4 shows a cross-section of the composite wafer of Figure 3, in a subsequent step of the manufacturing process;
- Figure 5 presents a detail of an alignment structure made on the wafer of Figure 1;
- Figure 6 presents a detail of a corresponding alignment structure made on the wafer of Figure 2;
- Figure 7 shows details of Figures 5 and 6 after alignment and bonding of the two substrates;
- Figure 8 is a top view of the alignment structure of Figure 5;
- Figure 9 is a perspective view of the step of aligning the structures of Figures 5 and 6;
- Figure 10 shows a cross-section of a first MEMS device formed using the parallel fabrication technique according to the invention;
- Figure 11 shows a cross-section of a second MEMS device formed using the parallel fabrication technique according to the invention;
- Figure 12 shows a cross-section of a third MEMS device formed using the parallel fabrication technique according to the invention;
- Figures 13-15 show cross-sections of a first wafer used for manufacturing the third MEMS device according to Figure 11, in successive steps; and
- Figure 16 shows a cross-section of a composite wafer obtained by bonding the wafer of Figure 15 to a wafer housing interconnections, in an advanced manufacturing step.

[0012] Figure 1 shows a cross-section of a first wafer 1 housing electronic components belonging to an integrated electronic circuit. In particular, the first wafer 1 comprises a substrate 2 having a surface 2a and housing a bipolar transistor 3 and a PMOS transistor 4, each formed in an own well 5, 6 isolated from one another by junction isolation regions 7. The well 5 accommodates a collector contact region 10 and a base region 11, and the base region 11 houses a base contact region 12 and an emitter region 13. The well 6 accommodates source regions 14. In addition, isolation contact regions 15 are formed inside the junction isolation region 7. The collector contact region 10, base region 11, base contact region 12, emitter region 13, source regions 14, and isolation contact regions 15 face the surface 2a of the substrate 2. A dielectric protection layer 18 extends on top of the surface 2a of the substrate 2 and has openings 19 at the regions 10, and 12-15. A gate region 20, of polycrystalline silicon, extends in part on top of the surface 2a and in part in a depression inside the substrate 2, and is electrically insulated from the substrate 2 by the dielectric protection layer 18.

[0013] The first wafer 1 is obtained via standard process steps, which are not described in detail herein.

[0014] Figure 2 shows a cross-section of a second wafer 25 comprising interconnection regions intended for the first wafer 1 of Figure 1. In particular, the second wafer 25 comprises a substrate 26 of monocrystalline silicon, covered by an oxide layer 27. Two metal levels are formed on top of the oxide layer 27 and comprise first connection regions 28 on top of the oxide layer 27 and second connection regions 30 on top of the first connection regions 28 and insulated therefrom by an insulating layer 31. Through connections 29 extend through the insulating layer 31 and selectively connect some of the first connection regions 28 to some of the second connection regions 30. Plug elements 32 are formed on top of the second connection regions 30 at the openings 19 and the gate region 20 of the first wafer 1. The plug elements 32 preferably comprise a base region 33, for example of aluminum, and a bonding region 34, of a metal capable of reacting with silicon to form a silicide, such as titanium, palladium, nickel, platinum, tungsten, and cobalt.

[0015] The second wafer 25 is preferably obtained as follows: initially the oxide layer 27 is deposited or grown on top of the substrate 26; then a first metal layer is deposited and defined so as to form the first connection regions 28; the insulating layer 31 is deposited; openings are formed in the insulating layer 31 where the through connections 29 are to be made; a second metal layer is deposited and removed from on top of the insulating layer 31; then a third metal layer is deposited and defined so as to form the second connection regions 30; next, a fourth metal layer and a metal layer capable of reacting with silicon are deposited and defined so as to form the plug elements 32. The first and second connection regions 28, 30 and the through connections 29 are made of any suitable metal, even one not necessarily compatible with processing of silicon, such as silver and copper.

[0016] Next (Figure 3), the second wafer 25 is turned upside down on top of the wafer 1 so that the top ends of the plug regions 32 insert into the corresponding openings 19, and, by applying an appropriate temperature (of at least 230°C, according to the type of metal capable of reacting with silicon) and a small pressure, the bonding regions 34 are made to react with the uncovered silicon through the openings 19 or with the polycrystalline silicon of the gate region 20 to form metal silicide which is conductive and stable over time. In this way, a composite wafer 36 is formed.

[0017] In order to guarantee the reaction of the bonding regions 34, the silicon exposed at the openings 19 and the polycrystalline silicon of the gate region 20 are preferably cleaned with gaseous anhydrous hydrofluoric acid, and all the silicon regions that are bonded to the plug regions (regions 10 and 12-15, and portion of the gate region 20 on which the contact is made) are on the same level.

[0018] Finally (Figure 4), the second wafer 25 is thinned, for example by lapping, by removing the substrate 26 as far as the oxide layer 27; then the oxide layer 27 is opened in order to enable selective connection of some of the first connection regions 28 with the outside. Alternatively, it is possible to thin the second wafer 25 to arrive near to the oxide layer 27, without, however, reaching the latter. Then, in the remaining portion of the substrate 26, openings are formed at the pads and traverse also the oxide layer 27, and connection wires are then bonded.

[0019] The gap between the first wafer 1 and the second wafer 25 forms an insulation gap 37 having a low dielectric constant and is filled with air or nitrogen, or else is set in vacuum conditions (in the latter two cases, bonding may be performed in a controlled environment as regards gas/pressure, and annular plug elements 32 may be provided which surround the active regions of each device into which the composite wafer 36 will then be divided, so as to seal the insulation gap 37 of each device from the external environment).

[0020] The advantages of the above described process are illustrated hereinafter. First, parallel processing allows a reduction in the cycle time, since the steps for manufacturing the second wafer can be carried out even simultaneously with, or in any case independently of, the steps for processing the first wafer.

[0021] Since the plug elements 32 belonging to the second wafer 25 are bonded directly to silicon regions belonging to the first wafer 1, the metallurgical operations for forming the connection regions are completely independent of the operations necessary for processing silicon; consequently, there is no interference whatsoever between such operations.

[0022] The areas in which the two wafers are made may be separate; consequently, for forming the connec-

tions it is possible to use materials that are incompatible with silicon processing, without any risk of contamination.

[0023] As far as the interconnections are concerned, it is possible to proceed from the simpler levels (top levels) to the more complex levels (bottom levels, including the first level which is connected directly to silicon), so increasing the sturdiness of the processes.

[0024] According to another aspect of the invention, in order to facilitate alignment of the second wafer 25 to the first wafer 1, self-alignment structures are made, as is shown in Figures 5-9, where only one portion of the wafers 1, 25 is illustrated.

[0025] In detail (Figures 5 and 6), the self-alignment structures comprise engagement seats 40 formed in the first wafer 1 and engagement elements 41 formed on the second wafer 25.

[0026] Specifically, as may be better seen from Figures 8 and 9, an engagement seat 40 comprises a guide opening 42 in the protective dielectric layer 18, having a trapezium shape, and a notch 43 in the substrate 2, also having a trapezium shape and with the minor base and the legs substantially aligned, respectively, to the minor base and part of the legs of the guide opening 42. The guide opening 42 has a much greater length (height of the trapezium) than the notch 43.

[0027] The engagement seats 40 are obtained as follows: using an appropriate mask or the mask for digging in the silicon used to form the depression 21, the notch 43 is initially dug; then, simultaneously and using the same mask as for the openings 19, the guide opening 42 is dug. In this way, the guide opening 42 is positioned precisely with respect to the openings 19.

[0028] The engagement elements 41 preferably include two pins 44 for each engagement seat 40, as may be seen in detail in Figures 8 and 9. The two pins 44 are arranged adjacent each other and have dimensions and position such as to engage a corresponding notch 43. The two pins 44 of each engagement element 41 are formed on top of a second connection region (which, in actual fact, does not have any function of electrical connection), and each of them comprises a bottom region 45, which may be made of any suitable material (for example, but not necessarily, of the same material as the base regions 33 of the plug elements 32), an intermediate region 46, formed together with and made of the same material as the base regions 33, and a top region 47, formed together with and made of the same material as the bonding regions 34.

[0029] Since the pins 44 comprise one region more than the plug elements 32, namely, the bottom region 45, they have a greater height than the plug elements 32 themselves, namely by an amount corresponding to the thickness of the bottom region 45.

[0030] The pins 44 are preferably formed as follows: a raising layer is deposited on top of the second connection regions 30 and is then removed everywhere, except where the pins 44 are to be formed, using an appropriate mask. In this step, raising regions are formed having dimensions that may not even coincide with those of the bottom regions 45, but may be of larger dimensions, in particular if the material of the bottom regions 45 is the same as that of the intermediate regions 46.

[0031] Next, the fourth metal layer and the metal layer capable of reacting with silicon are deposited and defined, so as to form simultaneously the plug elements 32 and the intermediate regions 46 and top regions 47. If the material of the raising regions is the same as the fourth metal layer, also the bottom regions 45 are defined in this step, even though this is not always indispensable.

[0032] When the second wafer 25 is turned upside down on top of the first wafer 1, it is roughly aligned in order to insert the pins 44 into the guide openings 42 next to the major bases of the trapeziums, as shown in Figure 8 with a solid line, and in Figure 9. Next, the second wafer 25 is displaced laterally with respect to the first wafer 1 in the direction indicated by the arrows A, until the pairs of pins 44 insert into the corresponding notches 43, thus causing the second wafer 25 to collapse towards the first wafer 1 and the plug elements 32 to engage the corresponding openings 19. Preferably, the height of the pins 44 and the depth of the notches 43 is chosen in such a way that the pins 44 do not touch the bottom of the notches 43, so as to guarantee that, even in the presence of process imprecisions, the plug elements 32 are always and securely in contact with the substrate 2 and the gate region 20 of the first wafer 1.

[0033] Lateral movement of the second wafer 25 ends when the two pins 44 of each engagement element 41 both interfere with the legs of the guide openings 42 and possibly of the notches 43, fittedly engaged, as shown by the dashed lines in Figure 8, and so guaranteeing excellent alignment of the wafers 1 and 25.

[0034] Figure 10 shows a device 50 formed by a first chip 51 housing a micro-electromechanical structure 61 and a second chip 52 housing electrical connection regions.

[0035] In detail, the first chip 51 comprises a first substrate 54 of monocrystalline silicon, a first insulating layer 55, for example of silicon dioxide, and an epitaxial layer 56 of polycrystalline silicon. The epitaxial layer 56 houses the micro-electromechanical structure 61, including a rotor 57, a stator 58, and biasing regions 59. The first insulating layer 55 has been removed from beneath the rotor 57 where an air gap 60 is formed in order to enable movement of the rotor 57, which is supported by spring elements (not shown) in a per se known manner.

[0036] The second chip 52 comprises a second substrate 65, of monocrystalline silicon, a second insulating layer 66, of silicon dioxide, a third insulating layer 67, of silicon nitride, and plug elements 68, each of which includes a base region 69, for example of aluminum, and a bonding region 70, of silicide, such as titanium silicide,

palladium silicide, nickel silicide, platinum silicide, tungsten silicide, and cobalt silicide.

[0037] The second substrate 65 has through openings 74 at some plug elements 68. Underneath the through openings 74 also the second insulating layer 66 and the third insulating layer 67 are removed. Thereby, the corresponding base regions 69 are accessible from behind and are connected to electrical connection wires 75 soldered through a gold ball (gold-wire bonding technique).

[0038] The device 50 is formed as follows: the first insulating layer 55 is deposited or grown on a first wafer of crystalline silicon (forming the first substrate 54); next, a thin layer of polycrystalline silicon is deposited, and an epitaxial layer 56 is grown. Alternatively, it is possible to use a SOI wafer. Using a trench mask, micro-electromechanical structures 61 are defined; then the first insulating layer 55 is removed from beneath the rotor 57.

[0039] Separately, the second insulating layer 66 is deposited or grown on a second silicon wafer (forming the substrate 65). The third insulating layer 67 is deposited. Using an appropriate mask, openings are formed in the third insulating layer 67. Then a metal layer, for example of aluminum, is deposited and defined to form the base regions 69. A layer of a metal capable of reacting with silicon is deposited and defined to form the bonding regions 70. Possibly, using an appropriate etching technique, the base regions 69 and the bonding regions 70 can be defined together using a single mask. Next, using an appropriate mask, positioning structures, for example notches, are formed on the rear of the second wafer, i.e., on the side opposite that on which the second insulating layer 66 and the third insulating layer 67 have been formed.

[0040] Subsequently, the second wafer is turned upside down on the first wafer, using the positioning structures present on the rear of the second wafer and possibly exploiting the technique of precise self-alignment described with reference to Figures 6-9. Subsequently, by heating to an appropriate temperature and applying a small pressure, the bonding regions 70 are soldered on the corresponding regions (here, the stator 58 and the biasing regions 59) of the micro-electromechanical structures 61, forming metal silicide. The second wafer is thinned, for example by milling, down to a thickness of between 50 and 100 μm, and, using an appropriate mask, the through openings 74 are formed. Then the portions of the second insulating layer 66 at the through openings 74 are removed, thus uncovering from the rear the base regions 69, which must be accessible for bonding. The composite wafer thus obtained is then cut into dice and positioned where required, and the electrical connection wires 75 are soldered.

[0041] Figure 11 shows a device 80 including a first chip 81, similar to the first chip 51 of Figure 10 (and hence its parts are designated by the same reference numbers and will not be further described herein), and a second chip 82 housing electrical connection regions obtained using the technique of silicon plugs.

[0042] The second chip 82 comprises a silicon substrate 83 accommodating through connection regions 84, having conductivity N^+ and insulated from the rest of the substrate 83 by annular insulation regions 85 of silicon dioxide. A top silicon layer 86 covers the rear of the substrate 83, and a bottom oxide layer 87 covers the front of the substrate 83. Plug regions 68, similar to the plug regions 68 of Figure 10, join the second chip 82 to the first chip 81. Some of the plug regions 68 are in electrical contact with the through connection regions 84 and extend through corresponding openings present in the bottom oxide layer 87.

[0043] Electrical connection regions 90, for example of aluminum, extend over of the top oxide layer 86 and are in electrical contact with the through connection regions 84 through openings made in the top oxide layer 86. A protection layer 91, of silicon nitride, covers the electrical connection regions 90 and the top oxide layer 86, except for openings where electrical connection wires 92 are soldered to the electrical connection regions 90 through gold-wire bonding.

[0044] The device 80 is manufactured as described hereinafter. A first wafer, accommodating the first chip 81, is formed as described previously in connection with Figure 10. The second chip 82 is manufactured from a second wafer comprising a monocrystalline-silicon sacrificial substrate, the top oxide layer 86, and the substrate 83, for example a SOI wafer or a wafer obtained by epitaxial growth starting from a polysilicon germ layer deposited over the top oxide layer 86.

[0045] Using a deep trench mask, the substrate 83 is etched as far as the top oxide layer 86. Then an oxide layer is deposited and fills the trenches just obtained and forms the annular insulation regions 85 and the bottom oxide layer 87. After possible planarization of the bottom oxide layer 87, using an appropriate mask openings are formed in the bottom oxide layer 87, so as to uncover the substrate 83 at the through connection regions 84. Next, plug regions 68 are formed as described above. As previously, using an appropriate mask, positioning structures (notches) are made on the rear of the second wafer.

[0046] Next, the second wafer is turned upside down, aligned and bonded to the first wafer, as above described, for example in a controlled environment. Subsequently, the second wafer is thinned by completely removing the sacrificial layer until the top oxide layer 86 is uncovered. Using an appropriate mask, openings are formed in the top oxide layer 86. A metal layer, for example of aluminum, is deposited and defined to form electrical connection regions 90. The protection layer 91 is deposited and defined. The wafer is cut into dice, and the electrical connection wires 92 are formed. Alternatively, deep trenches are formed in the second wafer and are filled with insulating material deposited to form the annular insulation regions 85 and the bottom oxide layer 87. The second wafer is turned upside down and bond-

ed to the first wafer; then it is reduced in thickness until the annular insulation regions are reached from the rear. Next, the top oxide layer 86, the electrical connection regions 90, and the protection layer 91 are formed. Finally, the composite wafer is cut into dice, and the electrical connection wires 92 are made.

[0047] Figure 12 shows a device 100 including a first chip 101, similar to the first chip 51 of Figure 10 (and hence its parts are designated by the same reference numbers and will not be further described herein), and a second chip 102 housing electrical connection regions which are directly accessible. The first chip 101 has a smaller area than the second chip 102, so that the chip 102 projects on one side beyond the first chip 101.

[0048] The second chip comprises a substrate 103 coated with an insulating layer 104, for example of silicon dioxide. Connection regions 105 belonging to a same metal level extend inside the insulating layer 104. Plug elements 68, similar to the plug elements of Figure 10, are formed on the surface of the insulating layer 104; some of them being in electrical contact, through the base region 69, with the connection regions 105. The plug elements 68 guarantee bonding between the first chip 101 and the second chip 102, as shown in Figures 10 and 11. In addition, a contact region 106 is present on the surface of the insulating layer 104, in the area that is not covered by the first chip 101 and is connected to a respective connection region 105 to enable connection with the outside world.

[0049] The device 100 of Figure 12 is manufactured as illustrated in Figures 13-16. As for the device 50 of Figure 10, a first wafer 110 comprises a sandwich of the substrate 54, the insulating layer 55, and the epitaxial layer 56. Next (Figure 14), after planarization of the surface of the epitaxial layer 56, for example by chemical-mechanical polishing (CMP), a trench mask 111 is deposited, and, using a blade, notches 112 are made in the first chip 101 starting from the surface of the epitaxial layer 56, through the insulating layer 55 and through most of the thickness of the substrate 54.

[0050] Next (Figure 15), the micro-electromechanical structures 61 are defined, and the first insulating layer 55 is removed from beneath the rotor 57 (to form an air gap 60) and from outside the biasing regions 59.

[0051] A second wafer 115 (Figure 16) is processed separately. In detail, on the substrate 103, a first oxide layer is initially deposited or grown; a metal layer is deposited and defined so as to form the connection regions 105; a second oxide layer is deposited so as to form, together with the first oxide layer, the insulating layer 104; the insulating layer 104 is opened to form vias; an aluminum layer is deposited and defined to form the base regions 69 and the contact regions 106; and a layer of a metal capable of reacting with silicon is deposited and defined to obtain the bonding regions 70.

[0052] Next (Figure 16), the first wafer 110 is turned upside down, aligned to the second wafer 115, and bonded as described above. Then the substrate 54 of the second wafer 110 is thinned. The composite wafer 116 thus obtained is cut into dice, and the external portions of the first wafer 110 are removed, exploiting the notches 112, to obtain the structure of Figure 12.

[0053] Finally, it is clear that modifications and variations may be made to the process and the devices described and illustrated herein, all falling within the scope of the invention, as defined in the attached claims. In particular, electronic components and/or micro-electromechanical systems may be integrated in the first wafer; and the second wafer may have any number of metal levels, from one up to five or six, according to the technology adopted and to the particular requirements.

Claims

1. A process for manufacturing an integrated device (36; 50, 80; 100), comprising the steps of:

   forming integrated structures (3, 4; 61) including semiconductor regions (10, 12-15, 20; 58, 59) and isolation regions (7, 18; 55) in a first wafer (1; 51; 81; 101) of semiconductor material;
   forming interconnection structures (28-30, 32; 68, 70; 84, 90, 91; 105, 106) of conductor material on a second wafer (25; 52; 82; 102) of semiconductor material;
   bonding said first wafer and said second wafer together,

   characterized in that said step of forming interconnection structures comprises forming plug elements (32; 68) having at least one bonding region (34; 70) of a metal material capable of reacting with said semiconductor regions (10, 12-15, 20; 58, 59) of said first wafer (1; 51; 81; 101), and said step of bonding said first wafer and said second wafer (1, 25; 51, 52; 81, 82; 101, 102) comprises causing said bonding region (34; 70) to react with said semiconductor regions.

2. The process according to Claim 1, wherein said semiconductor material is silicon, and said step of causing said bonding region (34; 70) to react comprises forming a metal silicide.

3. The process according to Claim 1 or Claim 2, wherein said metal material is chosen from among titanium, nickel, platinum, palladium, tungsten, and cobalt.

4. The process according to any of the preceding claims, wherein said plug elements (32) have a height, and said step of forming integrated structures (3, 4) comprises forming an insulating material layer (18) on top of a substrate (2) of semiconductor

material, said insulating material layer having a thickness smaller than said height of said plug elements (32), and forming openings (19) in said insulating material layer (18) to uncover selective portions of said substrate (2), and wherein said step of bonding said first and second wafers (1, 25; 51, 52; 81, 82; 101, 102) comprises causing said bonding region (34) to react with at least said selective portions (10, 12-15) of said substrate.

5. The process according to any of the foregoing claims, wherein said step of forming integrated structures (3, 4) comprises forming an insulating material layer (18) on top of a substrate (2) of semiconductor material, and forming conductive regions (20) of semiconductor material on top of said insulating material layer, and said step of bonding said first and second wafers (1, 25) comprises causing said bonding region (34) to react with said conductive regions (20).

6. The process according to any of the foregoing claims, wherein said step of forming interconnection structures comprises forming electrical connection regions (28-30; 75; 84, 90, 91; 105) of conductive material, and said step of forming plug elements (32; 68) comprises forming base regions (33; 69) of conductive material on top of and in direct electrical contact with said electrical connections regions, and forming said bonding regions (34; 70) on top of said base regions.

7. The process according to any of the foregoing claims, wherein said step of forming integrated structures comprises forming integrated electronic components (3, 4).

8. The process according to any of the foregoing claims, wherein said step of forming integrated structures comprises forming micro-electromechanical systems (61).

9. The process according to any of the foregoing claims, further comprising, before said step of bonding said first and second wafers (1, 25), the step of forming self-alignment structures (40, 41) on said first and second wafers, and aligning said first and second wafers, using said self-alignment structures.

10. The process according to Claim 9, wherein said step of forming self-alignment structures (40, 41) comprises forming at least one engagement seat (40) in one of said first and second wafers (1, 25), and forming at least one engagement element (41) on another of said first and second wafers (1, 25) in a position facing said engagement seat.

11. The process according to Claim 10, wherein said step of forming integrated structures (3, 4) comprises forming an insulating material layer (18) on top of a substrate (2) of semiconductor material, said step of forming at least one engagement seat (40) comprises forming a guide opening (42) in said insulating material layer, said guide opening (42) having a basically trapezium shape, with a major base and a minor base, and said engagement element (41) having transverse dimensions smaller than said major base and greater than said minor base, and said step of aligning said first and second wafers (1, 25) comprises inserting said engagement element (41) into said guide opening (42) near said major base and displacing said second wafer (25) with respect to said first wafer (1) so to bring said engagement element (41) towards said guide opening (42) until said engagement element (41) slots into said engagement seat (40).

12. The process according to Claim 11, wherein said step of forming at least one engagement seat (40) comprises forming a notch (43) in said substrate (2) beneath said guide opening (42), said step of forming an engagement element (41) comprises forming at least one pin element (44) of greater height than the thickness of said insulating material layer (18), and said step of displacing said second wafer (25) comprises causing said pin element (44) to snap into said notch (43) before fittedly engaging said engagement element (41) into said slotting seat (40).

13. An integrated device (36; 50, 80; 100) comprising:

a first body (1; 51; 81; 101) of semiconductor material housing integrated structures (3, 4; 61) including semiconductor regions (10, 12-15, 20; 58, 59) and isolation regions (7, 18; 55);
a second body (25; 52; 82; 102) of semiconductor material carrying interconnection structures (28-30, 32; 68; 90, 91; 105, 106) of conductive material;

characterized in that said bonding structures comprise plug elements (32; 68) in direct contact with said semiconductor regions (10, 12-15, 20; 58, 59) and having at least one bonding region (34; 70) of a material resulting from the reaction of said semiconductor regions with a metal material.

14. The device according to Claim 13, wherein said semiconductor material is silicon, and said material resulting from the reaction of said semiconductor regions (10, 12-15, 20; 58, 59) with a metal material is a metal silicide.

15. The device according to Claim 14, wherein said metal material is chosen from among titanium, nick-

el, platinum, palladium, tungsten, and cobalt.

16. The device according to any of Claims 13-15, wherein said plug elements (32) have a height, said first body (1) comprises an insulating material layer (18) on top of a substrate (2) of semiconductor material, said insulating material layer having a thickness smaller than the height of said plug elements (32), and openings (19) uncovering selective portions of said substrate (2), and wherein said bonding region (34) is bonded to said selective portions of said semiconductor regions (10, 12-15).

17. The device according to any of Claims 13-16, wherein said first body (1) comprises an insulating material layer (18) on top of a substrate (2) of semiconductor material and conductive regions (20) of semiconductor material on top of said insulating material layer, and wherein said bonding region (34) is bonded to said conductive regions (20).

18. The device according to any of Claims 13-17, wherein said integrated structures comprise integrated electronic components (3, 4).

19. The device according to any of Claims 13-17, wherein said integrated structures comprise microelectromechanical systems (61).

20. The device according to any of Claims 13-19, wherein said first body (1) and said second body (25) comprise self-alignment structures (40, 41).

21. The device according Claim 20, wherein said self-alignment structures comprise at least one engagement seat (40) in one of said first and second bodies (1, 25), and at least one engagement element (41) on another of said first and second bodies (1, 25) in a position facing said engagement seat.

22. The device according Claim 21, wherein said first body (1) comprises a substrate (2) of semiconductor material, an insulating material layer (18) on top of said substrate, at least one guide opening (42) in said insulating material layer, said guide opening (42) having a basically trapezium shape, with a major base and a minor base, and said engagement element (41) has transverse dimensions smaller than said major base and greater than said minor base and extending in said guide opening (42) in a position of interference with said engagement seat (40).

23. The device according Claim 22, wherein said insulating material layer (18) has a thickness, said substrate (2) has a notch (43) beneath said guide opening (42), and said engagement element (41) comprises at least one pin element (44) which has a greater height than the thickness of said insulating material layer (18) and extends at least partially inside said notch (43).

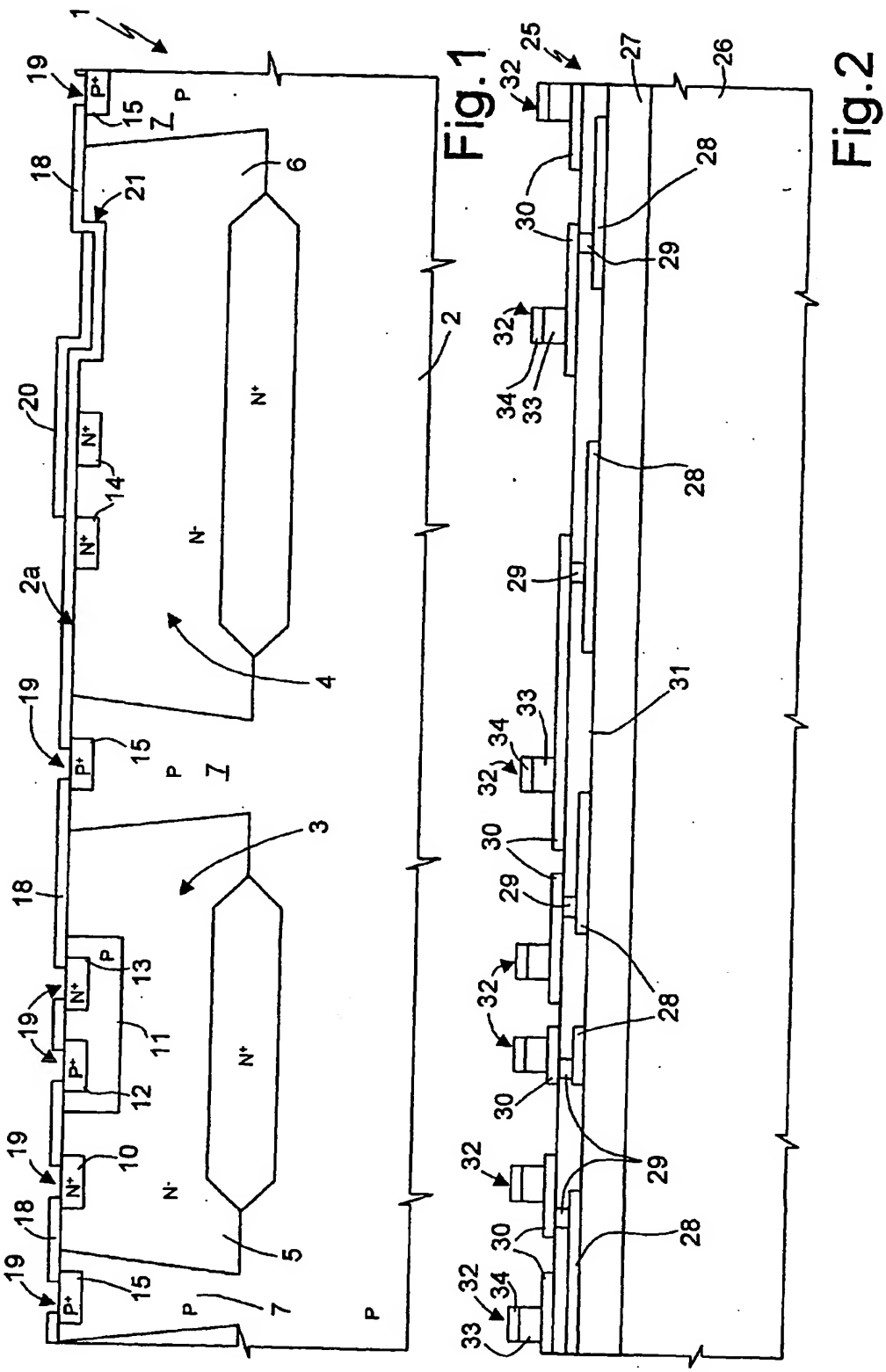
1
19
P+
15
P
18
21
6
20
N+
14
N+
2a
N-
4
19
P+
15
P
3
18
P
13
N+
19
11
P+
12
19
10
N+
N-
18
19
P+
15
P
7
P
5

Fig.1

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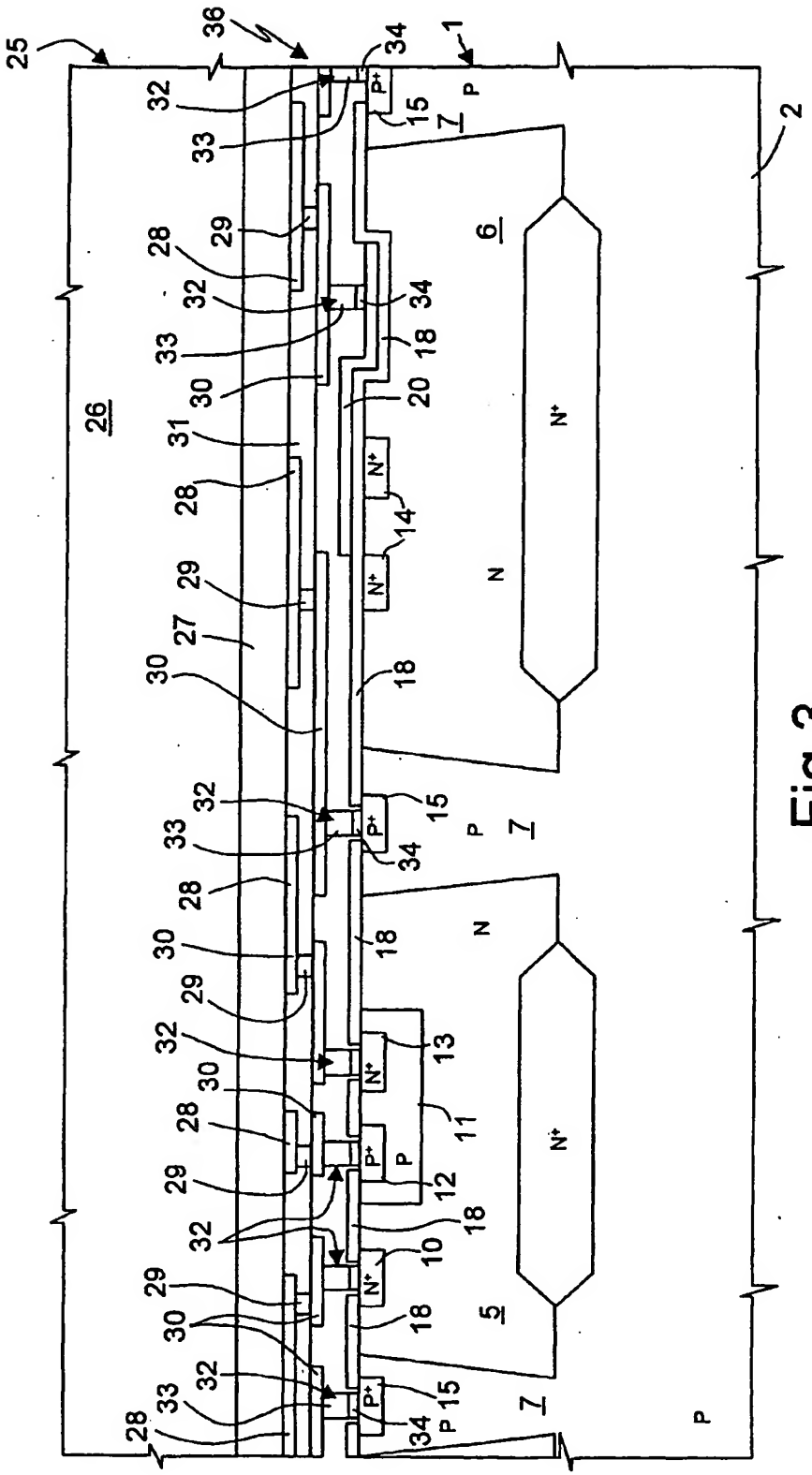
Fig.2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34
1
32
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15
P
7
2
28
29
6
32
34
33
18
30
20
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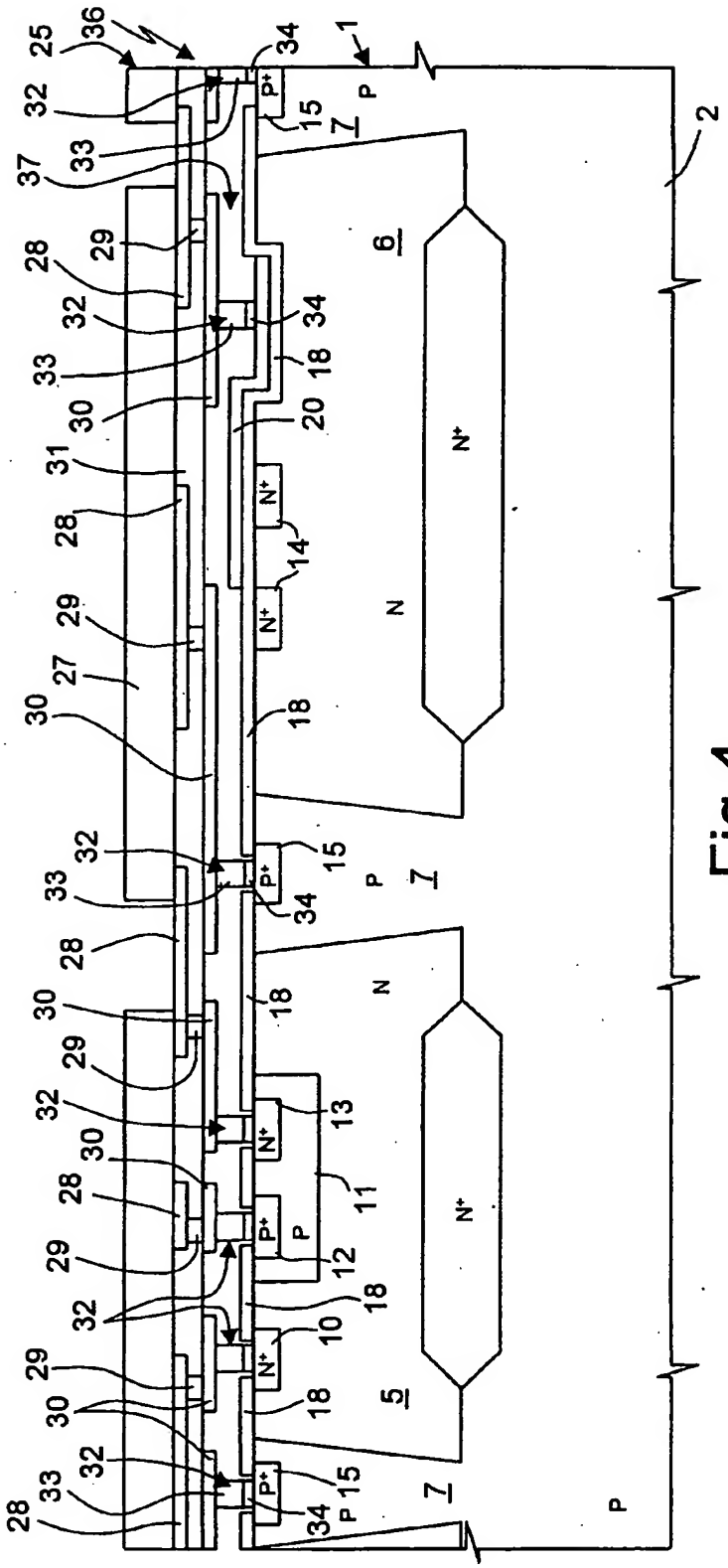
N+
28
14
N
29
27
30
18
32
15
33
P+
34
7
28
N
30
18
29
32
13
N+
30
28
11
P+
P
29
12
32
18
10
29
30
18
5
32
33
P+
15
28
34
P
7
P

Fig.3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36
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N+
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P+
34
P
7
28
N
30
18
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32
13
N+
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28
11
P+
P
29
12
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N+
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32
33
P+
15
28
34
P
7
P

Fig.4

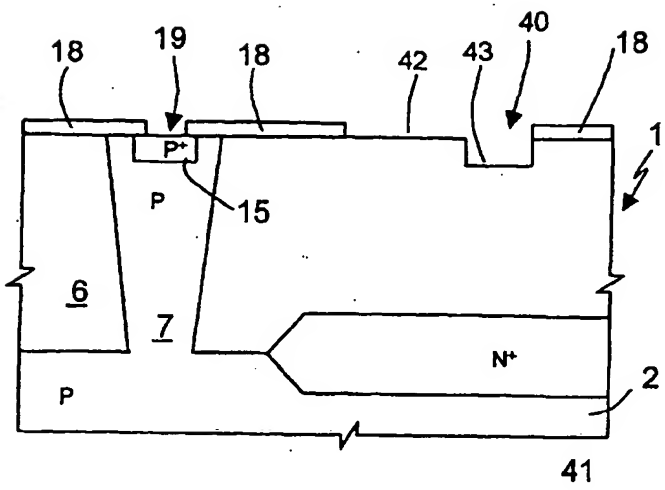

Fig.5

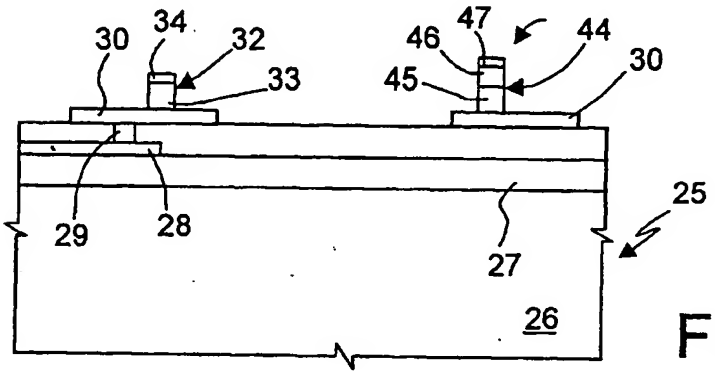

Fig.6

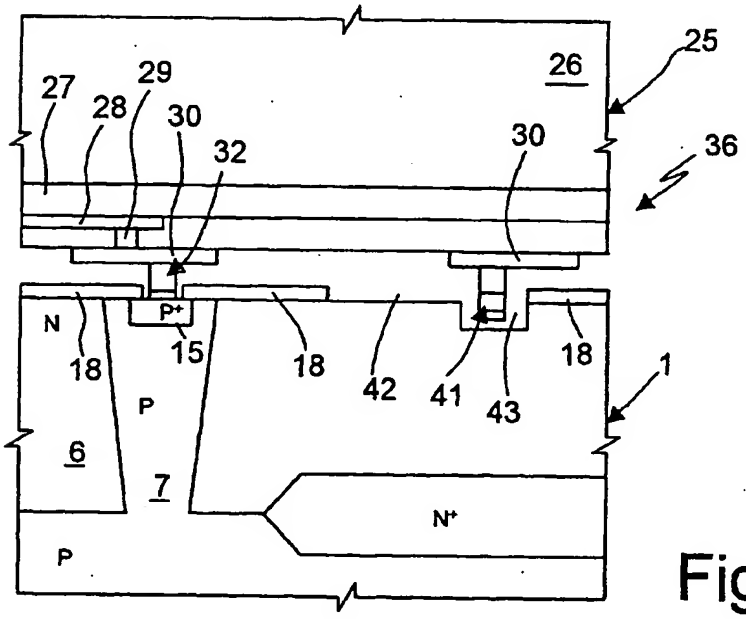

Fig.7

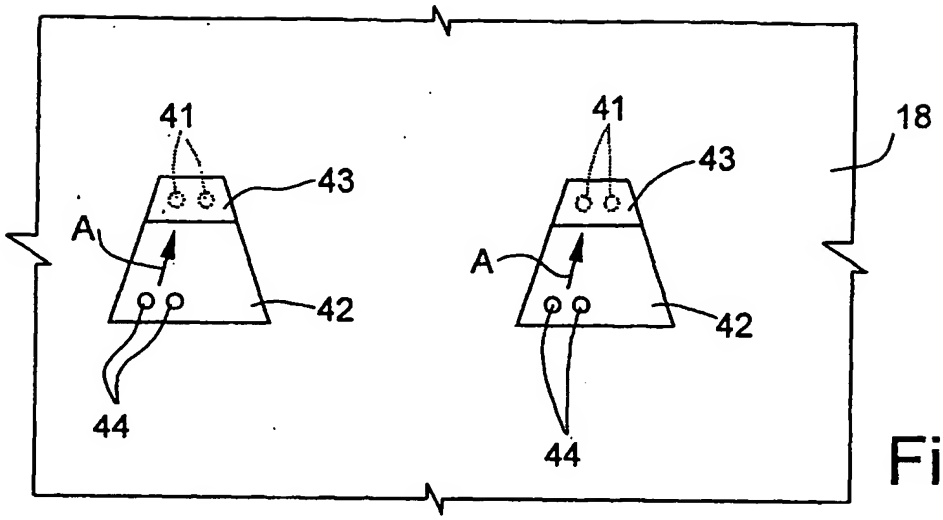

Fig.8

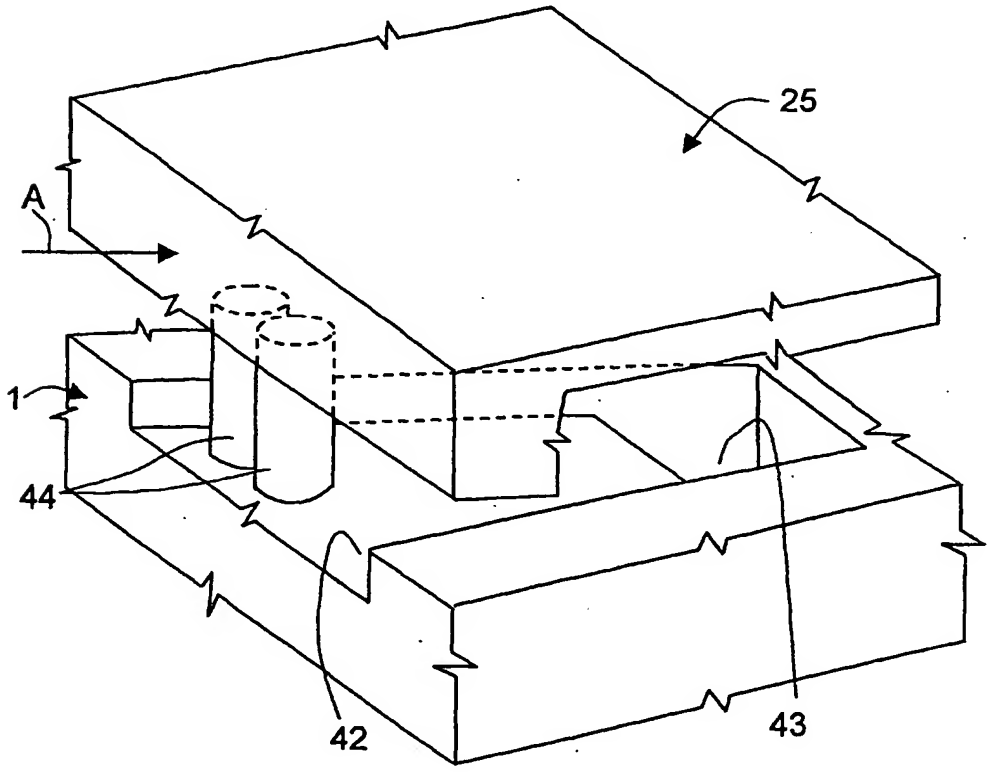

Fig.9

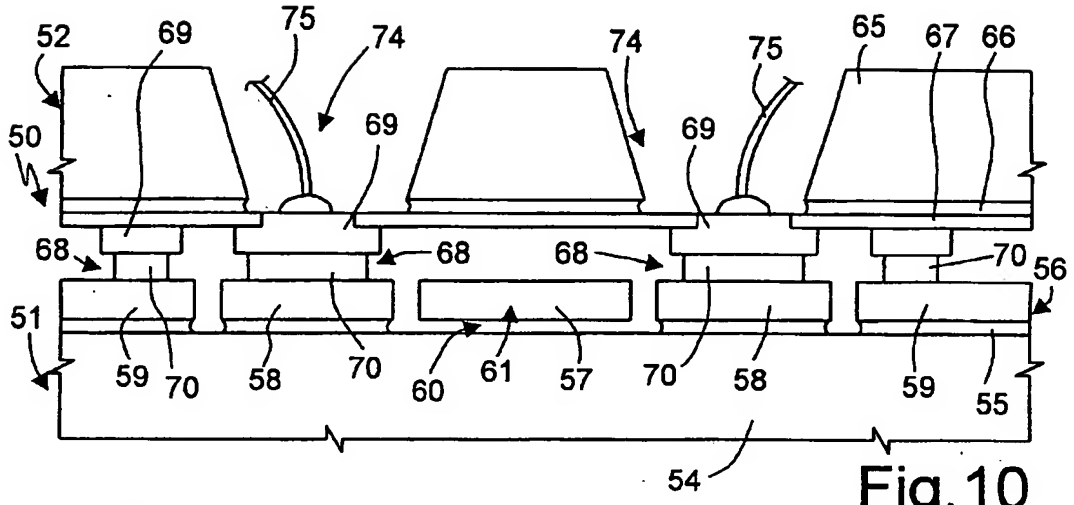

Fig.10

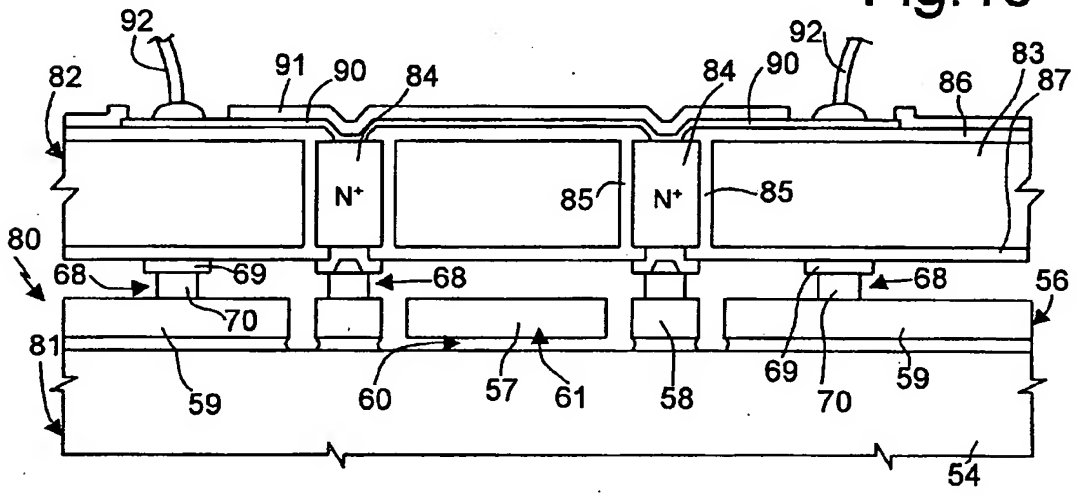

Fig.11

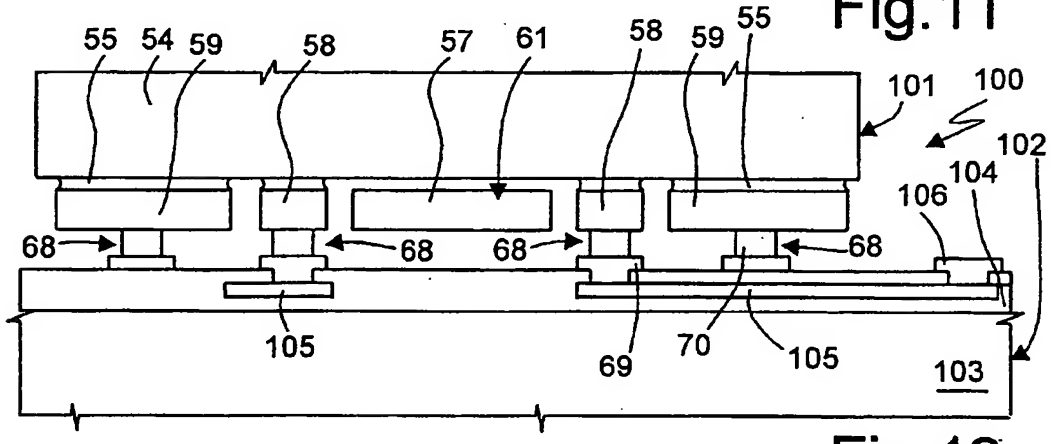

Fig.12

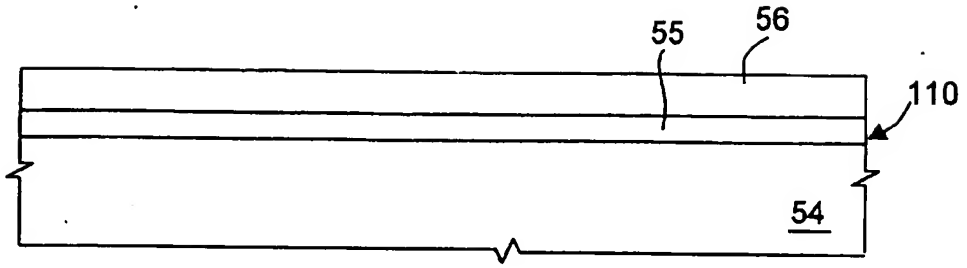

Fig.13

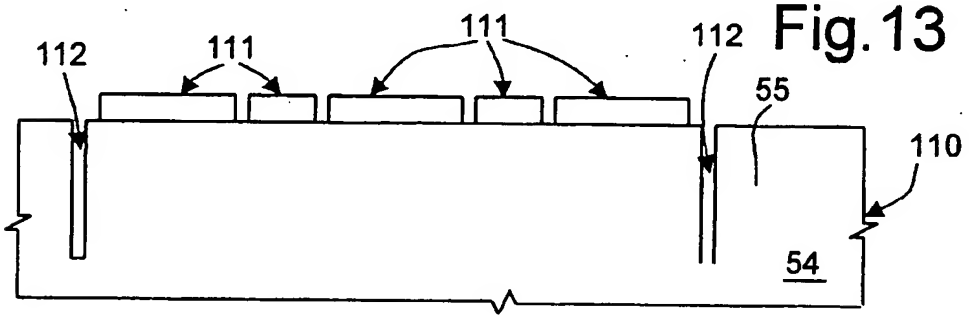

Fig.14

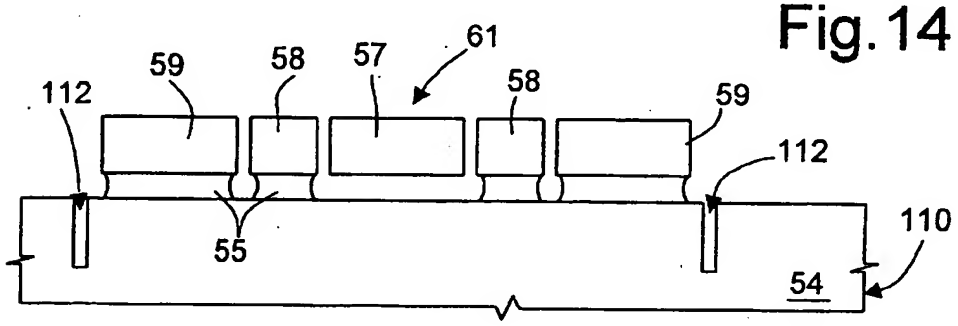

Fig.15

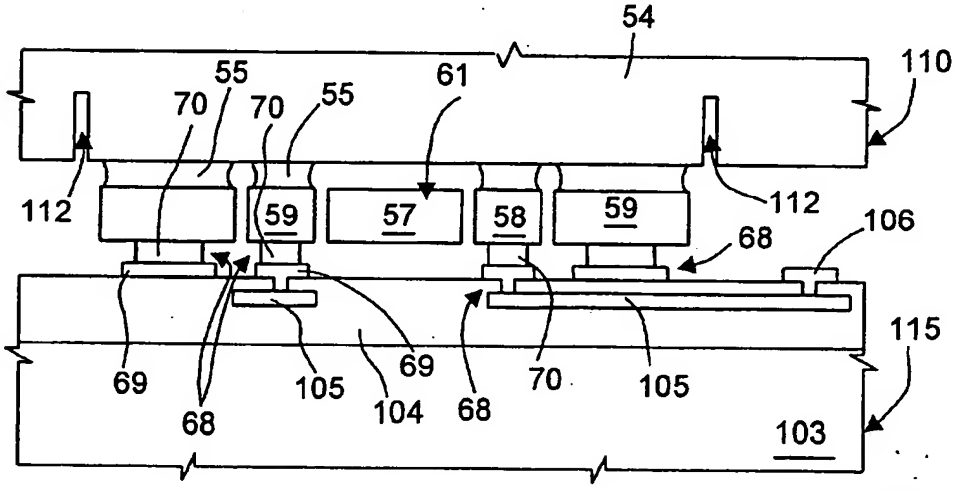

Fig.16

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 00 83 0867

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
Y	ISMAIL M S ET AL: "PLATINUM SILICIDE FUSION BONDING" ELECTRONICS LETTERS,GB,IEE STEVENAGE, vol. 27, no. 13, 20 June 1991 (1991-06-20), pages 1153-1155, XP000238688 ISSN: 0013-5194 * the whole document *	1-8,13, 19	B81C3/00 H01L21/98 H01L21/60
Y	EP 0 993 034 A (FORD MOTOR CO) 12 April 2000 (2000-04-12) * abstract; figure 3 *	1-8,13, 19	
Y	US 3 254 389 A (ANDRES ET AL.) 7 June 1966 (1966-06-07) * the whole document *	1-8,13, 19	
A	US 5 406 701 A (PEPE ANGEL A ET AL) 18 April 1995 (1995-04-18) * the whole document *	9-12, 20-23	
A	US 5 627 106 A (HSU CHEN-CHUNG) 6 May 1997 (1997-05-06) * figures 10-12 *	4-6,16, 17	TECHNICAL FIELDS SEARCHED (Int.Cl.7) B81C H01L
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A	US 5 858 814 A (GOOSSEN KEITH WAYNE ET AL) 12 January 1999 (1999-01-12)		

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	18 May 2001	Prohaska, G

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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